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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,779	11/04/2003	An-Chun Tu	TS03-268	5490
7590 07/30/2004				
STEPHEN B. ACKERMAN 28 DAVIS AVENUE POUGHKEEPSIE, NY 12603			EXAMINER NHU, DAVID	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/700,779

Applicant(s)

TU ET AL.

OK

Examiner

David Nhu

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.



Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

FINAL

DETAIL ACTIONS

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1-26 are rejected under U.S.C 103(a) as being unpatentable over Background of Invention (BOI) in view of Chan et al (6,252,277 B1).

Regarding claim 1, BOI, figure 1, pages 1-4, disclose a method of forming an interlevel dielectric (ILD) layer with improved gap filling comprising the steps of: providing a semiconductor substrate 10 having closely spaced gate electrodes 14; forming sidewall spacers 18 on said gate electrodes; forming source/drain contact areas 20 adjacent to said sidewall spacers; forming a metal silicide layer 22 on said gate electrodes and on said source/drain contact areas.

BOI fails to teach the steps of removing said sidewall spacers; forming said ILD layer over and between said gate electrodes and filling gaps between said gate electrodes on said substrate. However, Chan, (see col. 3, lines 14-16, figures 4J-4K, col. 6, lines 29-67), teach the steps of removing said sidewall spacers 35; forming said ILD layer 50 over and between said gate electrodes 44 and filling gaps 49 between said gate electrodes on said substrate 30.

Regarding claim 2, a polysilicon layer deposited to a thickness about 1500 and 1800 Angstroms (see Chan, col. 9, lines 15-18).

Art Unit: 2818

Regarding claim 3, the substrate includes lightly doped source and drain regions formed by ion implanting an N-type dopant for n-channel and ion implanting a P-type dopant for p-channel (see Chan, col. 7, lines 4-6, col. 8, lines 30-31, col. 10, lines 14-20).

Regarding claim 4, the sidewall spacers are formed by depositing a CVD insulating layer and anisotropically etching back to said substrate (see Chan, col. 7, lines 4-50).

Regarding claim 5, the source/drain contact areas are formed by ion implanting an N-type dopant for N-channel and ion implanting a P-type dopant for P-channel (see Chan, col. 7, lines 4-6, col. 8, lines 30-31, col. 10, lines 14-20).

Regarding claim 6, using a salicide process that uses a metal selected from the group that includes cobalt, nickel, and titanium (see Chan, col. 6, lines 35-36).

Regarding claim 8, using a hot phosphoric acid solution (see Chan, col. 6, lines 46-48).

Regarding claims 11, 12, the ILD layer by CVD to a thickness (see Chan, col. 6, lines 56-61).

Regarding claim 13, the ILD layer is a dielectric material having a low-dielectric constant (see BOI, page 2, line 8).

Regarding claim 14, **Regarding claim 1**, BOI, figure 1, pages 1-4, disclose a method of forming an interlevel dielectric (ILD) layer with improved gap filling comprising the steps of: providing a semiconductor substrate 10 having closely spaced gate electrodes 14; forming lightly doped source and drain regions 16 adjacent to said polysilicon gate electrodes 14; forming sidewall spacers 18 on said polysilicon gate electrodes; forming source/drain contact areas 20 adjacent to said sidewall spacers; forming a self-metal silicide layer 22 on said polysilicon gate electrodes and on said source/drain contact areas.

Art Unit: 2818

BOI fails to teach the steps of removing said sidewall spacers; forming said ILD layer over and between said gate electrodes and filling gaps between said gate electrodes on said substrate. However, Chan, (see col. 3, lines 14-16, figures 4J-4K, col. 6, lines 29-67), teach the steps of removing said sidewall spacers 35; forming said ILD layer 50 over and between said gate electrodes 44 and filling gaps 49 between said gate electrodes on said substrate 30.

Regarding claim 15, a polysilicon layer deposited to a thickness about 1500 and 1800 Angstroms (see Chan, col. 9, lines 15-18).

Regarding claim 16, the substrate includes lightly doped source and drain regions formed by ion implanting an N-type dopant for n-channel and ion implanting a P-type dopant for p-channel (see Chan, col. 7, lines 4-6, col. 8, lines 30-31, col. 10, lines 14-20).

Regarding claim 17, the sidewall spacers are formed by depositing a CVD insulating layer and anisotropically etching back to said substrate (see Chan, col. 7, lines 4-50).

Regarding claim 18, the source/drain contact areas are formed by ion implanting an N-type dopant for N-channel and ion implanting a P-type dopant for P-channel (see Chan, col. 7, lines 4-6, col. 8, lines 30-31, col. 10, lines 14-20).

Regarding claim 19, using a salicide process that uses a metal selected from the group that includes cobalt, nickel, and titanium (see Chan, col. 6, lines 35-36).

Regarding claim 21, using a hot phosphoric acid solution (see Chan, col. 6, lines 46-48).

Regarding claim 22, using in-situ plasma etching in a high-density plasma etcher (see Chan, col. 5, lines 7-27).

Regarding claims 24, 25, the ILD layer by CVD to a thickness (see Chan, col. 6, lines 56-61).

Art Unit: 2818

Regarding claim 26, the ILD layer is a dielectric material having a low-dielectric constant (see BOI, page 2, line 8).

It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Chan into BOI as both are related to the same subject matter of forming an ILD layer over a substrate having spaced gate electrodes, source/drain regions to sidewall spacers, metal silicides on the source/drain region and on gate electrodes; forming the ILD layer over and between gate electrodes and filling ILD into gaps.

Response to Arguments

3. Contrary to the applicant's argument about claims 1, 14, in his remarks, page 11, Chan does not describe/teach the sidewall spacers are removed before the IDL layer are deposited/formed. In fact, Chan clearly teaches "the spacer/sidewall is optionally removed and an ILD layer is deposited through which contacts to the device elements are formed". See Chan, figures 4J, 4K, col. 3, lines 14-16, col. 6, lines 47-63.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

Art Unit: 2818

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Buynoski'012 is cited as of interest.

6. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

David Nhu 

July 27, 2004

